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High-speed Data Acquisition Design Based on ZYNQ

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ABSTRACT
To address the demands for high-speed and high-precision data acquisition and calibration of Cherenkov light signals generated by SiPM(Silicon Photomultiplier) arrays in LACT (Large Array of Imaging Atmospheric Cherenkov Telescopes) cameras, this study designs a high-speed multi-channel data acquisition and calibration system based on ZYNQ. The FPGA's parallel processing capabilities enable rapid signal acquisition control, real-time calibration algorithms , and multi-channel synchronization coordination. A 250Mbps(mega samples per second) high-speed ADC(analog-to-digital converter) converts optoelectronic signals to digital format, while the system coordinates with LACT's main data link through high-speed interfaces like AXI-Stream for real-time calibration data storage and feedback. Experimental verification demonstrates that the system achieves dual-channel synchronized calibration with less than 0.1% error, ensuring consistent precision in LACT's gamma-ray detection across the 1TeV-1PeV energy range. The system exhibits strong real-time performance, high stability, and excellent adaptability.

KEYWORDS
High-speed data acquisition; High precision; ZYNQ-7000; AD9643

1 Introduction

Although LHAASO has achieved groundbreaking results in ultra-high-energy gamma-ray detection by discovering over 40 gamma-ray sources in the TeV energy range, its detection mode based on water Cherenkov detectors and scintillator arrays remains limited in angular resolution (approximately 0.1-0.5°) and detailed morphological characterization of extended sources. This limitation hinders in-depth research on radiation mechanisms and spatial distributions of high-energy gamma-ray sources above 10 TeV, particularly PeVatron particles. To address this, the LACT project was proposed. By deploying a 32-unit imaging atmospheric Cherenkov telescope array with angular resolution exceeding 0.05°, and leveraging the high sensitivity and multi-channel simultaneous detection capabilities of SiPM cameras, it fills the gap in high-precision ultra-high-energy gamma-ray observations in the Northern Hemisphere.

The detection performance of LACT cameras is highly dependent on the photoelectric response consistency of SiPM arrays. As the core front-end support, its calibration system requires precise calibration of 16×16 SiPM pixels. To address this, a ZYNQ-based data acquisition system was designed. The ZYNQ SOC integrates an ARM Cortex-A9 dual-core processor and Xilinx 7-series FPGA architecture(model: XC7Z010). The on-chip integration of highly customized AXI interconnects and interfaces serves as a bridge between components, accelerating communication between modules and enhancing system stability. Leveraging the FPGA's hardware programmability, an interface controller connected to high-speed ADCs was designed. By utilizing the official AXI DMA IP, collected data can be directly transferred to ARM's DDR for storage. ARM-powered Ethernet sends data to host software for comprehensive system decision-making. Through analysis of LED light signals converted by SiPM during LACT camera calibration, the nanosecond-level pulse width requires sufficient temporal resolution from the sampling system. The selected AD9643 acquisition card features 250MHz sampling frequency, four-channel synchronization, and 14-bit resolution, meeting both charge resolution (30% ±1 pe) and multi-channel synchronization requirements for accurate optoelectronic signal conversion. Compared to ZYNQ's built-in XADC with 12-bit width and 1MHz sampling rate, the AD9643 demonstrates superior temporal resolution and quantization accuracy, better suited for high-speed LED calibration signal acquisition.

2 Overall Design of Data Acquisition System

Figure 1 presents a schematic overview of the system design. The system begins by generating standardized optical signals using a tunable wavelength light source, which is matched to the 280–550 nm Cherenkov radiation band. These signals uniformly illuminate the SiPM camera through an optical system. The SiPM converts the optical signals into analog electrical signals, which are then digitized by the AD9643 high-speed ADC (14-bit resolution, 250 MSPS (mega samples per second) sampling rate). The ADC's high bandwidth enables it to capture the nanosecond-scale pulses output by the SiPM, ensuring quantization accuracy even for subtle variations in light intensity.

The digitized signals are then fed into the ZYNQ heterogeneous platform. Within the ZYNQ, the FPGA portion (PL) handles synchronized buffering and preprocessing of multi-channel data. The data is then transferred to the ARM portion (PS) via the AXI-DMA interface and subsequently uploaded to a host computer in real time through Gigabit Ethernet. On the host computer, SiPM gain calibration, dark current compensation, and channel consistency correction are performed based on the acquired data. The resulting calibration parameters are then fed back into the LACT main data chain,

thereby ensuring precise gamma-ray imaging by the telescope.

Through the closed-loop design of "light source, photoelectric conversion, high-speed digitization and real-time transmission", the calibration system makes up for the defects of low efficiency and poor environmental adaptability of traditional offline calibration, and provides a performance benchmark for front-end detection unit to achieve 0.05° angular resolution of LACT.

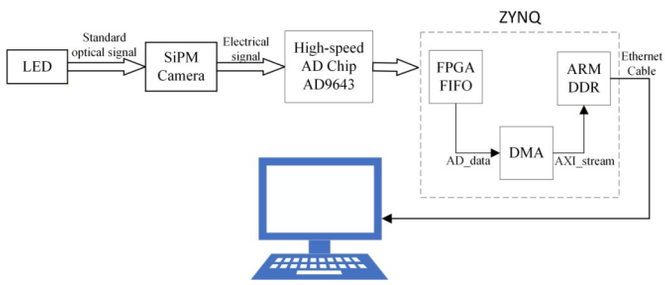

Figure 1 Overall design of data acquisition system

3 Hardware Design of Data Acquisition system

3.1 ZYNQ Introduction

ZYNQ is an all-programmable SoC (system-on-chip) developed by Xilinx, which innovatively integrates an ARM Cortex-A9 dual-core processor (PS component) with a Field-Programmable Gate Array (FPGA, PL component). The chip utilizes the AMBA AXI4 interconnect bus to efficiently interface with internal memory, external storage, and various peripherals including USB, Ethernet, SD, UART, HDMI, and GPIO ports[4-5]. With abundant logic resources (up to 6.25 MHz logic unit operation capacity) and a 766 MHz internal clock, it not only supports ARM-based system control and protocol processing but also enables hardware acceleration and flexible expansion through FPGA. This provides an integrated, highly modular hardware foundation for systems requiring real-time performance and high precision, finding extensive applications in industrial control, communication, image processing, and related fields.

3.2 AD9643 Controller Design

The AD9643, a high-performance high-speed ADC chip, offers 14-bit resolution and a 250 MSPS sampling rate. Its differential input voltage range of ±0.875 V matches the output amplitude of SiPM detectors, ensuring no signal clipping during photoelectric conversion. Additionally, Its differential input/output mode effectively suppresses common-mode interference, providing reliable hardware support for scenarios requiring precise signal acquisition and rapid response, such as LACT camera calibration systems.

The AD converter architecture is illustrated in Figure 2: its signal processing chain begins with single-ended analog electrical signals generated by an external SiPM converter, which first undergo front-end differential operational amplification and synchronization with a 1 V reference voltage to form differential voltage signals matching the AD9643's input range, then enter the AD9643 via the AD_data_P and AD_data_N differential input ports (providing 14 differential channels in total); external differential clock signals (clk_p and clk_n) are also supplied to the AD9643, whose differential clock signals output from DCO(Data Clock Output) ports are converted to single-ended clocks using the IBUFDS primitive (differential input buffer) , driving the IDDR(input double data rate) module to sample data from one channel on the rising clock edge and from a second channel on the falling clock edge for dual-channel parallel sampling; the digitized signals are then formatted into AXI4-Stream data and output via the M00_AXIS and M01_AXIS interfaces, with a FIFO(First-In-First-Out) buffer implemented at the ADC output for cross-clock domain synchronization to resolve frequency mismatches between the ADC sampling clock and AXI bus clock, and finally, the DMA(Direct Memory Access) controller ensures reliable data transfer to DDR memory to prevent data loss during high-speed acquisition.

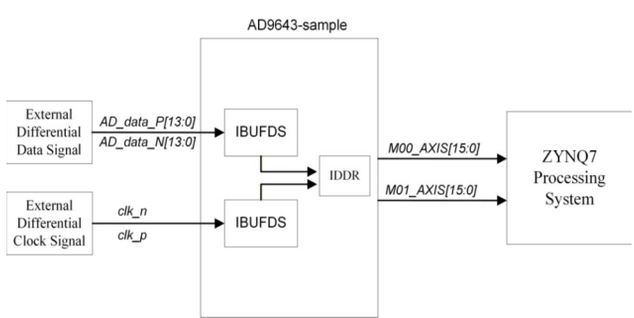

Figure 2 AD9643 port connection diagram

3.3 Acquisition System Communication

The system communication architecture combines "internal AXI bus interconnection with external Ethernet transmission". Internally, it utilizes the ZYNQ heterogeneous architecture. Calibrated data from AD9643 acquisition is transmitted unidirectionally to the PS-end DDR via the AXI-Stream interface and AXI-DMA hardware IP through the AXI bus write channel, adapting to cross-clock domain differences to ensure real-time performance. Externally, a link is established through the ZYNQ PS-end Ethernet interface. Using socket programming, the data in DDR is encapsulated into TCP packets for high-speed transmission to the host computer via Ethernet protocols. Compared to traditional UART, Ethernet offers 1Gbps bandwidth, 100-meter transmission distance, and error checking mechanisms, meeting the multi-channel, high-speed data feedback requirements of LACT camera calibration systems and providing reliable support for the "acquisition-calibration" closed-loop process.

3.4 DDR High-Speed Memory

The hardware configuration of DDR3 DRAM in this system takes advantage of the dual-edge sampling feature of dual-speed synchronous dynamic random-access memory (DDR)—it samples data during both rising and falling edges of clock cycles, which significantly boosts storage performance. Specifically, to ensure sufficient data throughput for high-speed acquisition, the system integrates two 4-Gbit DDR3 chips (model H5TQ4G63ARFR-PBC). With a 32-bit DDR bus width, this setup achieves peak operating speeds of up to 533 MHz. The DDR memory connects directly to ZYNQ's BANK502 memory interface. When configuring the memory in the ZYNQ Processing System core, it is critical to ensure that DDR interface models are identical or compatible—this guarantees reliable data transmission and overall system stability.

4 Software Design of Data Acquisition System

In the Xilinx IDE suite, after completing hardware engineering design in Vivado, the SDK automatically configures key parameters across three modules: Hardware Definition defines register types, address mappings, and IP block configurations; BSP (Board Support Package) contains driver programs and variable parameter header files for supported IP blocks; Application is used to test various functionalities. This configuration completes the system software design.

4.1 Trigger Acquisition Control Module

The host computer parses instructions based on specific communication protocols to determine triggering modes. The system is preset with four mutually exclusive operational modes: external triggering (instruction-triggered, SMA pulse-triggered, RS485 pulse-triggered) and internal threshold-triggered modes, ensuring conflict prevention for flexible adaptation to diverse LACT camera calibration scenarios. The instruction-triggered mode immediately initiates data acquisition after receiving commands, enabling precise human control of timing. The SMA pulse-triggered mode delays data collection by a predetermined duration after detecting rising edges of pulses, with each edge corresponding to a data packet for accurate synchronization with external SMA pulse signals. The RS485 pulse-triggered mode leverages the strong anti-interference capability and long-distance transmission capacity of RS485 bus, making it suitable for complex industrial environments or remote scenarios. The threshold-triggered mode continuously monitors signals, initiating data acquisition and packet generation when thresholds are exceeded, then immediately resumes monitoring upon data transmission completion while automatically capturing signals exceeding specified intensity levels. These four modes work together through rigorous recognition and response mechanisms to ensure precise and reliable collection of LACT camera calibration data.

4.2 ADC-DMA Control

In this system, the AXI-DMA controller serves as the core for data interaction between PL and PS ports in ZYNQ's heterogeneous architecture. It transmits high-speed data collected by the AD9643 acquisition module from the PL to DDR memory on the PS side. Utilizing the SG mode, the controller manages multiple non-contiguous DDR memory blocks through descriptor chain tables, enabling "one-time configuration, continuous transmission". Under SG mode, the controller first allocates independent memory blocks in DDR and creates a circular linked list by recording address and length information in the BD . After initiating transmission, the controller automatically completes data transfer in sequence according to the linked list. Upon completion of a memory block transfer, an interrupt is triggered. The PS-side processor then reads and uploads the data to the host computer while updating the BD status for the next transmission cycle. This mode avoids frequent CPU intervention, adapts to the AD9643's 250MSPS high-speed data stream, supports dynamic adjustment of memory block sizes for LED calibration pulse width matching, and ensures that errors in individual memory block transfers do not affect the entire link. This guarantees efficient and stable data transfer for LACT camera calibration while providing complete raw data for subsequent algorithms like SiPM gain calibration.

5 Experimental Result Analysis

A signal generator was used to provide the required signals for the experiment. Figure 3(a) presents the configuration of the signal generator; data acquisition was performed on 1 MHz, 1.75 Vpp sine wave signals (with amplitudes ranging from 40 mV to 1.79 V). The sampling frequency of the ADC was set to 250 MHz, and all four acquisition channels were activated. However, due to hardware limitations, only single-channel experiments were conducted (see Figure 3(b)).

The data received by the host computer is shown in Figure 3(c): the waveform displayed on the graphical interface matches the theoretical period of the 1 MHz signal (1 μs), and its sinusoidal oscillation pattern is consistent with the original signal output by the generator. This visually confirms the system's effectiveness in acquiring 1 MHz high-frequency sine waves under single-channel mode.

To further validate the acquisition accuracy, eight sets of simulated voltage values were tested under single-channel operation. The test results were output via the serial port, as listed in Table 1. The first row represents the reference voltages from the signal generator, while the second row shows the voltage values measured by the system. Using Equation (1), the acquisition error was calculated to be 0.02%.

$$\text{Measurement accuracy} = \frac{\text{Measured value} - \text{Reference value}}{\text{Reference value}} \tag{1}$$

a b c

Figure 3 Experimental results

(a) Signal generator setup (b) Test platform (c) Display results

Table 1 Data acquisition results

Benchmark(mV)	1790	1700	1405	700	500	450	180	40
CH(mV)	1789.60	1699.88	1404.93	700.31	500.1	449.87	179.97	40.015

6 Conclusions

To address the high-precision signal acquisition requirements for weak optoelectronic signals in the SiPM calibration of LACT cameras, we developed a high-speed data acquisition system based on the AD9643 chip on the ZYNQ SoC, using the Xilinx Vivado development kit. The hardware architecture leverages ZYNQ's FPGA module to control AD9643-based signal acquisition, while its ARM core enables data transmission through the AXI-HP high-speed interface, AXI-DMA core, and SG mode and additionally driving the HDMI interface for real-time signal display. The software configures BD packets under SG mode and controls DMA data transfer. Test results demonstrate that the system achieves an error rate of 0.02% for 1 MHz signal acquisition, featuring compact size, low power consumption, high precision, strong real-time performance, and stability—thus fully meeting the signal acquisition demands of SiPM calibration.

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